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ELECTRONIC INSTRUMENT AND SEMICONDUCTOR MEMORY DEVICE

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Respectfully submitted,

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SPECIFICATION

TO ALL WHOM IT MAY CONCERN:

BE IT KNOWN THAT WE, Takaaki Suzuki, a citizen of Japan residing at Kawasaki-shi, Kanagawa, Japan, Masao Taguchi, a citizen of Japan residing at Kawasaki-shi, Kanagawa, Japan and Kotoku Sato, a citizen of Japan residing at Kawasaki-shi, Kanagawa, Japan have invented certain new and useful improvements in

ELECTRONIC INSTRUMENT AND SEMICONDUCTOR MEMORY DEVICE

of which the following is a specification : -

TITLE OF THE INVENTION

ELECTRONIC INSTRUMENT AND SEMICONDUCTOR
MEMORY DEVICE

5 BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an electronic instrument having a semiconductor memory device for which read and write operations are 10 executed in synchronism with strobe signals, and the semiconductor memory device.

2. Description of the Related Art

A circuit configuration of a part of a conventional electronic instrument is shown in Fig. 15 1. Referring to Fig. 1, there is a DDR-SDRAM (Double Data Rate Synchronous Dynamic Random Access Memory) 1 which operates in synchronism with rising and falling edges of a clock signal. The actual 20 electronic instrument has a plurality of DDR-SDRAMs and a control chip controlling the plurality of DDR-SDRAMs.

The electronic instrument further has a positive-phase clock line 2, an inverse-phase clock line 3, a command bus 4, an address bus 5 and a data 25 bus 6. A positive-phase clock signal CLK is transmitted through the positive-phase clock line 2. An inverse-phase clock signal /CLK having a phase which is in inverse relation to the phase of the positive-phase clock signal CLK is transmitted 30 through the inverse-phase clock line 3. Command signals are transmitted through the command bus 4. Row address signals and column address signals are transmitted through the address bus 5. Data is transmitted through the data bus 6.

35 In addition, a strobe signal line 7 is provided in the electronic instrument. An output strobe signal QSOUT is transmitted to the control

chip through the strobe signal line 7 in a data read operation (a data output operation) for each of the plurality of DDR-SDRAMS (e.g., the DDR-SDRAM 1).
5 The output strobe signal QSOUT is supplied to the control chip together with output data DQOUT and used to appoint a take-in timing of the output data DQOUT. An input strobe signal QSIN is transmitted to the DDR-SDRAM 1 through the strobe signal line 7 in a data write operation (a data input operation)
10 for the DDR-SDRAM 1. The input strobe signal QSIN is supplied to the DDR-SDRAM 1 together with input data DQIN and used to appoint a take-in timing of the input data DQIN.

An essential part of the DDR-SDRAM 1 is
15 shown in Fig. 2. Referring to Fig. 2, the DDR-SDRAM 1 has a command buffer 9, a command decoder 10 and a controller 11. The command buffer 9 receives a command signal transmitted through the command bus 4. The command decoder 10 decodes the command signal
20 output from the command buffer 9. The controller 11 receives a decoded command signal from the command decoder 10 and controls an internal circuit of the DDR-SDRAM 1 in accordance with the contents of the decoded command signal.

The DDR-SDRAM 1 further has an address buffer 12, a plurality of memory banks 14-1 - 14-m and address latches 13-1 - 13-m. The address buffer 12 receives a row address signal and a column address signal transmitted through the address bus 5.
25 Each of the address latches 13-1 - 13-m latches the row address signal and column address signal output from the address buffer 12. The memory bank 14-1 has a memory array 15-1 in which memory cells are arranged, a row decoder 16-1, a sense-amp unit 17-1
30 and a column decoder 18-1. The row decoder 16-1 decodes the row address signal latched by the address latch 13-1 to select a word line. The
35

sense-amp unit 17-1 includes sense amplifiers amplify data read out from a memory cell specified by the selected word line. The column decoder 18-1 decodes the column address signal latched by the 5 address latch 13-1 to select a column. The other memory banks (14-m) have the same structure as the memory bank 14-1.

The DDR-SDRAM 1 has data bus buffers 19-1 - 19-m and write buffers 20-1 - 20-m. Each of the 10 data bus buffers 19-1 - 19-m amplifies read data output from a corresponding one of the memory banks 14-1 - 14-m to a corresponding one of core data buses CDB1 - CDBm. Each of the write buffers 20-1 - 20-m outputs write data to a corresponding one of 15 the core data buses CDB1 - CDBm.

The DDR-SDRAM 1 further has a data output buffer 21, a data input buffer 22, a strobe output buffer 23 and a strobe input buffer 24. A peripheral data bus DB connects the data bus buffers 20 19-1 - 19-m and the write buffers 20-1 - 20-m to the data output buffer 21 and the data input buffer 22. The data output buffer 21 outputs the output data DQOUT to the outside and the data input buffer 22 receives from the outside input data DQIN having N 25 bits arranged in parallel. The strobe output buffer 23 outputs the output strobe signal QSOUT. The strobe input buffer 24 receives the input strobe signal QSIN and is used to control a take-in timing of the input data DQIN.

30 Relationships among the complementary clock signals CLK and /CLK, the output strobe signal QSOUT and the output data DQOUT in the data output operation (the data read operation) for the DDR-SDRAM 1 are shown in Fig. 3. Referring to Fig. 3, a time tCKQS is a QS access time from an edge of the 35 clock signal CLK, and a time tQSPRE is a QS preamble time, a time tQSPOT is a QS postamble time. Further,

a time tQSQ is a data output skew from an edge of the output strobe signal QSOUT, a time tAC is a data access time from an edge of the output strobe signal QSOUT, and a time tDV is a data output valid time.

5 Relationships among the complementary clock signals CLK and /CLK, the input strobe signal QSIN and the input data DQIN in a data input operation (the data write operation) for the DDR-SDRAM 1 are shown in Fig. 4. Referring to Fig. 4, a
10 time tDS is a data input set up time, and a time tDH is a data input hold time from each edge of the input strobe signal QSIN.

In the electronic instrument having the above structure, the output strobe signal QSOUT is
15 transmitted from the DDR-SDRAM 1 through the strobe signal line 7 together with the output data DQOUT through the data bus 6 so that the settling period for the output data DQOUT on the basis of the output strobe signal QSOUT is constant. As a result, it is
20 easy for the control chip to receive the output data DQOUT. The input strobe signal QSIN is transmitted from the control chip through the strobe signal line 7 together with the input data DQIN through the data bus 6 so that the settling period the input data
25 DQIN on the basis of the input strobe signal QSIN is constant. As a result, it is easy for the DDR-SDRAM 1 to receive the input data DQIN.

However, if the rising time and falling time of each of the strobe signals QSOUT and QSIN
30 are varied, the strobe period is not constant. The settling period for the data DQOUT and DQIN is thus not constant. As a result, it is difficult to adjust the take-in timing of the data DQOUT and DQIN. If the strobe period is shortened to access the DDR-SDRAM 1 at a very high speed, for example, if the strobe period is equal to or less than 4 nanoseconds (ns), the data DQOUT and DQIN may not be certainly

settled.

SUMMARY OF THE INVENTION

Accordingly, a general object of the
5 present invention is to provide a novel and useful
electronic instrument and semiconductor memory
device in which the disadvantages of the
aforementioned prior art are eliminated.

A specific object of the present invention
10 is to provide an electronic instrument in which even
if the strobe period used to appoint the take-in
timing of the data is shortened to access the
semiconductor memory device at a very high speed,
the data can be certainly settled.

15 The above objects of the present invention
are achieved by an electronic instrument comprising:
a memory device; clock lines through which
complementary clock signals are transmitted to be
used for synchronization of a data output operation
20 for the memory device; and strobe signal lines
through which a first output strobe signal and a
second output strobe signal are transmitted to be
used to settle output data from the memory device in
the data output operation, the first and second
25 output strobe signals being in complementary
relation to each other.

According to the present invention, even
if the rising time and falling time of each of the
first and second output strobe signals which are in
30 complementary relation to each other are varied, the
strobe period of the first and second output strobe
signals (the period between cross points of the
first and second output strobe signal) are constant.
As a result, the period in which the output data is
35 settled can be constant. Thus, even if the strobe
period used to appoint the take-in timing of the
output data is shortened to access the memory device

at a very high speed, the output data can be certainly settled.

The above objects of the present invention are also achieved by an electronic instrument comprising: a memory device; clock lines through which complementary clock signals are transmitted to be used for synchronization of a data input operation for the memory device; and strobe signal lines through which a first input strobe signal and 10 a second input strobe signal are transmitted to be used to settle input data supplied to the memory device in the data input operation, the first and second input strobe signals being in complementary relation to each other.

According to the present invention, even if the rising time and falling time of each of the first and second input strobe signals which are in complementary relation to each other are varied, the strobe period of the first and second input strobe 20 signals (the period between cross points of the first and second input strobe signal) are constant. As a result, the period in which the input data is settled can be constant. Thus, even if the strobe period used to appoint the take-in timing of the 25 input data is shortened to access the memory device at a very high speed, the input data can be certainly settled.

The above objects of the present invention are achieved by a semiconductor device provided in 30 an electronic instrument having clock lines through which complementary clock signals are transmitted to be used for synchronization of a data output operation for the semiconductor memory device, and strobe signal lines through which a first output 35 strobe signal and a second output strobe signal are transmitted to be used to settle output data from the semiconductor memory device in the data output

operation, the first and second output strobe signals being in complementary relation to each other, the semiconductor memory device comprising: a data output buffer that outputs the output data from 5 a memory bank; and a strobe output buffer that generates the first and second output strobe signals based on a predetermined signal, the first and second output strobe signals being supplied from the strobe output buffer to the strobe signal lines when 10 the output data is output from the data output buffer.

Further, the above objects of the present invention are achieved by a semiconductor memory device provided in an electronic instrument having 15 clock lines through which complementary clock signals are transmitted to be used for synchronization of a data input operation for the semiconductor memory device, and strobe signal lines through which a first input strobe signal and a 20 second input strobe signal are transmitted to be used to settle input data supplied to the semiconductor memory device in the data input operation, the first and second input strobe signals being in complementary relation to each other, the 25 semiconductor memory device comprising: a strobe input buffer that receives the first and second input strobe signals transmitted through the strobe signal lines and generates a strobe clock signal based on the first and second input strobe signals; 30 and a data input buffer that receives input data items supplied to the semiconductor memory device, the input data items being settled by using the clock strobe signal generated by the input strobe buffer.

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BRIEF DESCRIPTION OF THE DRAWINGS

Other objects, features and advantages of

the present invention will be apparent from the following description when read in conjunction with the accompanying drawings, in which:

5 Fig. 1 is a circuit diagram illustrating a part of a conventional electronic instrument;

Fig. 2 is a circuit diagram illustrating a DDR-SDRAM provided in the electronic instrument;

10 Fig. 3 is a timing chart illustrating signals and output data in a data output operation;

Fig. 4 is a timing chart illustrating signals and input data in a data input operation;

Fig. 5 is a circuit diagram illustrating a part of an electronic instrument according to an embodiment of the present invention;

15 Fig. 6 is a circuit diagram illustrating an essential part of an FCRAM provided in the electronic instrument shown in Fig. 5;

Fig. 7 is a circuit diagram illustrating a data output buffer and a strobe output buffer both of which are provided in the FCRAM shown in Fig. 6;

20 Fig. 8 is a circuit diagram illustrating a data input buffer and a strobe input buffer both of which are provided in the FCRAM shown in Fig. 6;

Fig. 9 is a timing chart illustrating signals and output data in a data output operation;

25 Fig. 10 is a timing chart illustrating an example of setting the level of complementary output strobe signals in a preamble time period in the data output operation for the FCRAM shown in Fig. 6;

30 Fig. 11 is a timing chart illustrating an example of setting the level of the complementary output strobe signals in a waiting time period of the FCRAM shown in Fig. 6;

Fig. 12 is a timing chart illustrating another example of setting the level of the complementary output strobe signals in the waiting time period of the FCRAM shown in Fig. 6;

Fig. 13 is a timing chart illustrating a relationship between a cross point of the complementary output strobe signals and a center point of a valid time period of the output data;

5 Fig. 14 is a timing chart illustrating signals and input data in the data input operation;

Fig. 15 is a timing chart illustrating an example of setting the level of complementary input strobe signals in the preamble time period in the
10 data input operation;

Fig. 16 is a timing chart illustrating an example of setting the level of the complementary input strobe signals in a waiting time period of a control chip;

15 Fig. 17 is a timing chart illustrating another example of setting the level of the complementary strobe signals in the waiting time period of the control chip; and

20 Fig. 18 is a timing chart illustrating a relationship between a cross point of the complementary input strobe signals and a center point of a valid time of the input data.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

25 A description will be given, with reference to the drawings, of an embodiment of the present invention.

A part of an electronic instrument according to an embodiment of the present invention
30 is formed as shown in Fig. 5. Referring to Fig. 5, there is an FCRAM (First Cycle Random Access Memory)
26 which is one type of the DDR-SDRAM. The FCRAM 26 is an embodiment of the semiconductor memory device according to the present invention. The actual
35 electronic instrument has a plurality of FCRAMS having the same structure and a control chip controlling the plurality of FCRAMS.

The electronic instrument has a positive-phase line 27, an inverse-phase line 28, a command bus 29, a address bus 30 and a data bus 31. A positive-phase clock signal CLK is transmitted through the positive-phase line 27. An inverse-phase clock signal /CLK having a phase which is in inverse relation to the phase of the positive-phase clock signal CLK is transmitted through the inverse-phase line 28. Command signals are transmitted through the command bus 29. Row address signals and column address signals are transmitted through the address bus 30. Data is transmitted through the data bus 31.

The electronic instrument further has a positive-phase strobe line 32 and an inverse-phase strobe line 33. A positive-phase output strobe signal QSOUT which is output from each of the FCRAMs (e.g., the FCRAM 26) together with output data DQOUT is transmitted to the control chip through the positive-phase strobe line 32. The positive-phase output strobe signal QSOUT is used to appoint the take-in timing of the output data DQOUT. A positive-phase input strobe signal QSIN which is output from the control chip together with input data DQIN is transmitted to each of the FCRAMs through the positive-phase strobe line 32. The positive-phase input strobe signal QSIN is used to appoint the take-in timing of the input data DQIN. An inverse-phase output strobe signal /QSOUT has a phase which is in inverse relation to the phase of the positive-phase output strobe signal QSOUT. The inverse-phase output strobe signal /QSOUT output from each of the FCRAMs (e.g., the FCRAM 26) is transmitted to the control chip through the inverse-phase strobe line 33. An inverse-phase input strobe signal /QSIN has a phase which is in inverse relation to the phase of the positive-phase input

strobe signal QSIN. The inverse-phase input strobe signal /QSIN output from the control chip is transmitted to each of the FCRAMs through the inverse-phase strobe line 33.

5 An essential part of each of the FCRAMs (e.g., the FCRAM 26) is formed as shown in Fig. 6. Referring to Fig. 6, the FCRAM 26 has a command buffer 35, a command decoder 36, an address buffer 37, a plurality of memory banks 39-1 - 39-m and
10 address latches 38-1 - 38-m. The command buffer 35 receives a command signal transmitted through the command bus 29. The command decoder 36 decodes the command signal output from the command buffer 35. The address buffer 37 receives a row address signal
15 and a column address signal both of which are transmitted through the address bus 30. Each of the address latches 38-1 - 38-m is coupled to one of the memory banks 39-1 - 39-m. Each of the address latches 38-1 - 38-m latches the row address signal
20 and the column address signal.

The memory bank 39-1 has a memory cell array 40-1, a row decoder 41-1, a sense-amp unit 42-1, a column decoder 43-1 and an active pre-controller 44-1. Plurality of memory cells are
25 arranged in the memory cell array 40-1. The row decoder 41-1 decodes the row address signal latched by the address latch 38-1 to select a word line. In the sense-amp unit 42-1, sense amplifiers amplify data read out from a memory cell which is selected
30 by the selected word line are arranged. The column decoder 43-1 decodes the column address signal latched by the address latch 38-1 to select a column. The active pre-controller 44-1 receives a decoded command signal from the command decoder 36 so as to
35 control the column decoder 43-1 and the sense-amp unit 42-1 in accordance with the contents of the command.

The other memory banks (39-m) have the same structure as the memory bank 39-1.

A burst length specifying a number corresponding to a plurality of data items (bits) 5 can be set in the FCDRAM 26. In such a case, a plurality of data items are read out from a selected memory bank in parallel in the data read operation, and a plurality of data items are written in a selected memory bank in parallel.

10 The FCRAM 26 has data bus buffers 45-1 - 45-m and write buffers 46-1 - 46-m. Each of the data bus buffers 45-1 - 45-m is coupled to a corresponding one of the memory banks 39-1 - 39-m and amplifies read data output from the 15 corresponding one of the memory banks 39-1 - 39-m to a corresponding one of core data buses CDB1 - CDBm. Each of the write buffers 46-1 - 46-m is coupled to a corresponding one of the memory banks 39-1 - 39-m and outputs write data to a corresponding one of the 20 core data buses CDB1 - CDBm.

The FCRAM 26 further has a parallel-to-serial converter 47, a data output buffer 48, a data input buffer 49, a serial-to-parallel converter 50, a strobe output buffer 51 and a strobe input buffer 25 52. The parallel-to-serial converter 47 converts parallel data transmitted from one of the data bus buffers 45-1 - 45-m which one corresponds to a selected memory bank into serial data. The data output buffer 48 outputs to the outside the serial 30 data DQOUT1-DQOUTN, formed of N bits, supplied from the parallel-to-serial converter 47. The data input buffer 49 receives input data DQIN1-DQINN, formed of N bits, supplied from the outside. The serial-to-parallel converter 50 converts the input data DQIN1- 35 DQINN from the data input buffer 49 into parallel data. The strobe output buffer 51 outputs the positive-phase output strobe signal QSOUT to the

positive-phase strobe signal line 32 and outputs the inverse-phase output strobe signal /QSOUT to the inverse-phase strobe signal line 33. The strobe input buffer 52 receives the positive-phase input strobe signal QSIN transmitted through the positive-phase strobe signal line 32 and receives the inverse-phase input strobe signal /QSIN transmitted through the inverse-phase strobe signal line 33.

The data output buffer 48 and the strobe output buffer 51 are formed as shown in Fig. 7. Referring to Fig. 7, an internal clock generator 100 generates an internal clock signal mCLK based on a clock signal supplied to the FCRAM 26. An internal output strobe signal generator 200 generates an internal output strobe signal mQSOUT based on a strobe signal supplied to the FCRAM 26. The internal clock signal mCLK generated by the internal clock generator 100 and a data enable signal DE are supplied to the data output buffer 48.

The data output buffer 48 has a nMOS transistors 54 and 55, an inverter 56, pMOS transistors 57 and 58, a latch circuit 59 and a latch circuit 62. The nMOS transistors 54 and 55 are on-and-off controlled by the internal clock signal mCLK. The inverter 56 inverts the internal clock signal mCLK. The pMOS transistors 57 and 58 are on-and-off controlled by an inverted internal clock signal from the inverter 56. The latch circuit 59 is formed of inverters 60 and 61 and latches the data enable signal DE. The latch circuit 62 is formed of inverters 63 and 64 and latches the output from the latch circuit 59. The output signal from the latch circuit 62 is input to one of two ports of each of NAND gates 65-1 - 65-N. Each of internal data items mDQOUT1 - mDQOUTN is input to another one of the two ports of a corresponding one of the NAND gates 65-1 - 65-N. An

output port of each of the NAND gates 65-1 - 65-N is connected to a corresponding one of three-state inverters 66-1 - 66-N. When the data enable signal DE is valid (has a high level) and the internal
5 clock mCLK has a high level, the signal latched by the latch circuit 59 has a low level and the signal latched by the latch circuit 62 has a high level. In this state, the internal output data items mDQOUT1 - mDQOUTN pass through the NAND gates 65-1 - 65-N
10 and are output as the output data items DQOUT1 - DQOUTN from the three-state inverters 66-1 - 66-N.

The strobe output buffer 51 has NAND gates 67 and 69, an inverter 68 and three-state inverters 70 and 71. The data enable signal DE is input to
15 one of two input ports of each of the NANG gates 67 and 69. The internal output strobe signal mQSOUT is input to another one of the input ports of the NAND gate 67. The internal output strobe signal mQSOUT is inverted by the inverter 68 and the output signal from the inverter 68 is input to another one of the input ports of the NAND gate 69. The output signal from each of the NAND gates 67 and 69 is input to a corresponding one of the three-state inverters 70 and 71. When the data enable signal DE is valid
20 (has a high level), the internal output strobe signal mQSOUT passes through the NAND gate 67 and is output as the positive-phase output strobe signal QSOUT from the three-state inverter 70. In addition, when the data enable signal DE is valid, the output signal from the inverter 68 passes through the NAND gate 69 and is output as the inverse-phase output strobe signal /QSOUT from the three-state inverter 71.
25 Thus, the positive-phase output strobe signal QSOUT and the inverse-phase output strobe signal /QSOUT are in inverse relation to each other.
30
35

The data input buffer 49 and the strobe input buffer 52 are formed as shown in Fig. 8.

Referring to Fig. 8, the strobe input buffer 52 has differential amplifiers 73 and 74. The positive-phase input strobe signal QSIN is input to a non-inverting terminal (+) of the differential amplifier 73 and an inverting terminal (-) of the differential amplifier 74. The inverse-phase input strobe signal /QSIN is input to an inverted terminal (-) of the differential amplifier 73 and a non-inverting terminal (+) of the differential amplifier 74. A strobe clock signal QS-CLK is obtained at a node at which output terminals of the differential amplifiers 73 and 74 are connected.

The data input buffer 49 has a plurality of synchronous flip flops (SFFs) 75-1 - 75-N. Each of the synchronous flip flops 75-1 - 75-N latches a corresponding one of the input data items DQIN1 - DQINN in synchronism with the strobe clock signal QS-CLK supplied from the strobe input buffer 52.

Fig. 9 shows a relationship among the complementary clock signals CLK and /CLK, the complementary output strobe signals QSOUT and /QSOUT, and output data items RD1 and RD2, which are consecutive two bits (DQOUT=RD1 and RD2), in the data output operation for the FCRAM 26. In the present embodiment shown in Fig. 9, a constant time period before the head of a cross point train of the complementary output strobe signals QSOUT and /QSOUT is set as the preamble time tQSPRE. The head of the cross point train corresponds to a start of a strobe period of the complementary output strobe signals QSOUT and /QSOUT. In the preamble time tQSPRE, the positive-phase output strobe signal QSOUT is controlled to be in a low level and the inverse-phase output strobe signal /QSOUT is controlled to be in a high level. These levels are set by use of the read command RD-CMD as a trigger.

In a case where a circuit has differential

amplifiers which receive the positive-phase output strobe signal QSOUT and the inverse-phase output strobe signal /QSOUT, an internal level of the circuit is controlled by respectively setting the
5 positive-phase output strobe signal QSOUT and the inverse-phase output strobe signal /QSOUT at the above levels in the preamble time tQSPRE. As a result, the circuit is controlled to be in a state where the output data DQOUT can receive.

10 In addition, a constant time period after a cross point of the complementary output strobe signals QSOUT and /QSOUT which cross point is the end of a period of the complementary output strobe signals QSOUT and /QSOUT is set as the postamble
15 time tQSPST. In this time period, the levels of the positive-phase output strobe signal QSOUT and the inverse-phase output strobe signal /QSOUT differ from each other.

In a period of waiting time other than the
20 preamble time tQSPRE, the output strobe valid time, a period of input strobe signal and the postamble time tQSPST, transistors of the FCRAM 26 which transistors drive the positive-phase strobe signal line 32 and the inverse-strobe signal line 33 are
25 controlled to be in an off state. As a result, the positive-phase strobe signal line 32 and the inverse-phase strobe signal line 33 are in a floating state, such as a high impedance state (Hi-Z) or a low impedance state (Low-Z).

30 In addition, in the embodiment of the present invention, each cross point of the complementary output strobe signals QSOUT and /QSOUT is set at an edge trigger point of the output data DQOUT.

35 In a case where there is a data latency with respect to the read command RD-CMD, the levels of the complementary output strobe signals QSOUT and

/QSOUT in the preamble time tQSPRE may be set a predetermined time period before (e.g., one or half clock before) a first data item DQOUT=DR1 is output, as shown in Fig. 10.

- 5 In a case where a complementary output strobe signal line and a complementary input strobe signal line are separated from each other and an even number of consecutive output data items DQOUT are output, the levels of the complementary output
10 strobe signals QSOUT and /QSOUT may be controlled in the period of waiting time as shown in Fig. 11. That is, the positive-phase output strobe signal QSOUT and the inverse-phase output strobe signal /QSOUT may be respectively maintained at the low
15 level and the high level in the same manner as in the postamble time tQSPST. In this case, there is no problem to cause the control chip to be in the state where the control chip can receive the output data.
- 20 In addition, in a case where the complementary output strobe signal line and the complementary input strobe signal line are separated from each other and one or an odd number of consecutive data items DQOUT are output, the levels
25 of the complementary output strobe signals QSOUT and /QSOUT may be controlled in the period of waiting time as shown in Fig. 12. That is, the positive-phase output strobe signal QSOUT and the inverse-phase output strobe signal /QSOUT may be
30 respectively maintained at the high level and the low level in the same manner as in the postamble time tQSPST and restored at the start of the preamble time tQSPRE in the next data read operation. In this case, there is no problem to cause the
35 control chip to be in the state where the control chip can receive the output data.

In addition, each cross point of the

complementary output strobe signals QSOUT and /QSOUT may be set at a center point of a period of the output data DQOUT as shown in Fig. 13.

Fig. 14 shows a relationship among the
5 complementary clock signals CLK and /CLK, the
complementary input strobe signals QSIN and /QSIN
and input data items W1 and W2, which are
consecutive two bits (DQIN =W1 and W2), in the data
input operation for the FCRAM 26. In the present
10 embodiment shown in Fig. 14, a constant time before
the head of a cross point train of the complementary
input strobe signals QSIN and /QSIN is set as the
preamble time tQSPRE. In the preamble time tQSPRE,
the positive-phase input strobe signal QSIN is
15 controlled to be in a low level and the inverse-
phase input strobe signal /QSIN is controlled to be
in a high level. These levels are set by use of the
write command WR-CMD as a trigger.

In a case where a circuit has differential
20 amplifiers which receive the positive-phase input
strobe signal QSIN and the inverse-phase input
strobe signal /QSIN, an internal level of the
circuit is controlled by respectively setting the
positive-phase input strobe signal QSIN and the
25 inverse-phase input strobe signal /QSIN at the above
levels in the preamble time tQSPRE. As a result,
the circuit is controlled to be in a state where the
input data DQIN can receive.

In addition, a constant time period after
30 a cross point of the complementary input strobe
signals QSIN and /QSIN which cross point is the end
of a period of the complementary input strobe
signals QSIN and /QSIN is set as the postamble time
tQSPOT. In this time period, the levels of the
35 positive-phase output strobe signal QSIN and the
inverse-phase input strobe signal /QSIN differ from
each other.

In a period of waiting time, transistors of the control chip which transistors drive the positive-phase strobe signal 32 and the inverse-phase strobe signal line 33 are controlled to be in
5 an off state. As a result, the positive-phase strobe signal line 32 and the inverse-phase strobe signal line 33 are in a floating state, such as a high impedance state (Hi-Z) or a low impedance state (LOW-Z).

10 In addition, in the embodiment of the present invention, each cross point of the complementary input strobe signals QSIN and /QSIN is set at an edge trigger point of the input data DQIN.

15 In a case where there is a data latency with respect to the write command WR-CMD, the levels of the complementary input strobe signals QSIN and /QSIN in the preamble time tQSPRE may be set a predetermined time period before a first data item DIN=WD1 is output, as shown in Fig. 15.

20 In a case where a complementary output strobe signal line and a complementary input strobe signal line are separated from each other and an even number of consecutive input data items DQIN are input, the levels of the complementary input strobe
25 signals QSIN and /QSIN may be controlled in the period of waiting time as shown in Fig. 16. That is, the positive-phase input strobe signal QSIN and the inverse-phase input strobe signal /QSIN may be respectively maintained at the low level and the
30 high level in the same manner as in the postamble time tQSPST. In this case, there is not problem to cause the FCRAM to be in the state where the FCRAM can receive the input data.

35 In addition, in a case where the complementary output strobe signal line and the complementary input strobe signal line are separated from each other and one or an odd number of

consecutive data items DQIN are input, the levels of the complementary input strobe signals QSIN and /QSIN may be controlled in the period of waiting time as shown in Fig. 17. That is, the positive-phase input strobe signal QSIN and the inverse-phase input strobe signal /QSIN may be respectively maintained at the high level and the low level in the same manner as in the postamble time tQSPST and restored at the start of the preamble time tQSPRE in the next data write operation. In this case, there is no problem to cause the FCRAM to be in the state where the FCRAM can receive the input data.

In addition, each cross point of the complementary input strobe signals QSIN and /QSIN may be set at a center point of a period of the input data DQIN as shown in Fig. 18.

As has been described above, in the electronic instrument according to the embodiment of the present invention, a set of the complementary output strobe signals QSOUT and /QSOUT is used as the output strobe signal. Thus, even if the rising time and falling time of the complementary output strobe signals QSOUT and /QSOUT are varied, the period of the complementary output strobe signals QSOUT and /QSOUT (a period between cross points of the complementary output strobe signals) can be constant. As a result, the period in which the output data DQOUT is settled can be constant.

In addition, a set of the complementary input strobe signals QSIN and /QSIN is used as the strobe signal. Thus, even if the rising time and falling time of the complementary input strobe signals QSIN and /QSIN are varied, the period of the complementary input strobe signals QSIN and /QSIN (the period between cross points of the complementary input strobe signals) can be constant. As a result, the period in which the input data DQIN

is settled can be constant.

According to the electronic instrument of the embodiment of the present invention, even if the strobe period is shortened, for example, if the 5 strobe period is equal to or less than 4 nanoseconds (ns), the data DQOUT and DQIN can be certainly transmitted and received.

In addition, in the FCRAM 26, data having a bit length corresponding to a burst length is read 10 out, as parallel data, from the selected bank. The data is converted into serial data by the parallel-to-serial converter 47. The serial data is then supplied to the data output buffer 48. As a result, the data read operation can be performed at a high 15 speed. Since the period of the complementary output strobe signals QSOUT and /QSOUT is constant so that the period in which the output data DQOUT is settled is constant, the parallel-to-serial converter 47 can have a margin for the operation.

20 In addition, in the FCRAM 26, the serial-to-parallel converter 50 is provided next to the data input buffer 49 and input data items DQIN (bits) corresponding to the burst length are successively supplied from the data input buffer 49 25 to the serial-to-parallel converter 50. The input data items DQIN are converted into parallel data by the serial-to-parallel converter 50 and the parallel data is written in the selected memory bank. As a result, the data write operation can be performed at 30 a high speed. Since the period of the complementary input strobe signals QSIN and /QSIN is constant so that the period in which the input data DQIN is settled is constant, the serial-to-parallel converter 50 can have a margin for the operation.

35 The present invention is not limited to the aforementioned embodiments, and other variations and modifications may be made without departing from

the scope of the claimed invention.

WHAT IS CLAIMED IS:

5

1. An electronic instrument comprising:
a memory device; and
strobe signal lines through which a first
output strobe signal and a second output strobe
10 signal are transmitted in synchronism with output
data from said memory device in the data output
operation, the first and second output strobe
signals being in complementary relation to each
other.

15

2. The electronic instrument as claimed
20 in claim 1, wherein said memory device has a strobe
output buffer that generates the first and second
output strobe signals based on a predetermined
signal, the first and second output strobe signals
being supplied from said strobe output buffer to
25 said strobe signal lines when the output data is
output from said memory device.

30

3. The electronic instrument as claimed
in claim 1, wherein the first and second output
strobe signals have different levels in a preamble
time which is a time period before a head of a cross
35 point train of the first and second output strobe
signals, the head of the cross point corresponding
to a start of a strobe period of the first and

second output strobe signals.

5

4. The electronic instrument as claimed in claim 3, wherein the first and second output strobe signals have different levels in a postamble time which is a time period after a cross point of
10 the first and second output strobe signals which cross point corresponds to an end of a strobe period of the first and second output strobe signals.

15

5. The electronic instrument as claimed in claim 3, wherein the levels of the first and second output strobe signals in the preamble time
20 are set by use of a read command as a trigger.

25

6. The electronic instrument as claimed in claim 3, wherein the levels of the first and second output strobe signals in the preamble time are set a predetermined time before a first output data item is output.

30

7. The electronic instrument as claimed in claim 6, wherein transistors of said memory device which transistors drive the strobe signal lines are controlled to be in a off state in a

waiting time period.

5

8. The electronic instrument as claimed
in claim 1, wherein each of cross points of the
first and second output strobe signals is set at an
edge trigger point of a corresponding one of output
10 data items.

15

9. The electronic instrument as claimed
in claim 1, wherein each of cross points of the
first and second output strobe signals is set at a
center point of a corresponding one of output data
items.

20

25

10. An electronic instrument comprising:
a memory device; and
strobe signal lines through which a first
input strobe signal and a second input strobe signal
are transmitted in synchronism with input data
supplied to said memory device in the data input
30 operation, the first and second input strobe signals
being in complementary relation to each other.

35

11. The electronic instrument as claimed
in claim 10, wherein said memory device has a strobe

input buffer that receives the first and second
input strobe signals transmitted through said strobe
signal lines and generates, based on the first and
second input strobe signals, a strobe clock signal
5 used to settle input data items supplied to said
memory device.

10

12. The electronic instrument as claimed
in claim 10, wherein the first and second input
strobe signals have different levels in a preamble
time which is a time period before a head of a cross
15 point train of the first and second input strobe
signals, the head of the cross point corresponding
to a start of a strobe period of the first and
second input strobe signals.

20

13. The electronic instrument as claimed
in claim 12, wherein the first and second input
25 strobe signals have different levels in a postamble
time which is a time period after a cross point of
the first and second input strobe signals which
cross point corresponds to an end of a strobe period
of the first and second input strobe signals.

30

14. The electronic instrument as claimed
35 in claim 12, wherein the levels of the first and
second input strobe signals in the preamble time are
set by use of a write command as a trigger.

15. The electronic instrument as claimed
in claim 12, wherein the levels of the first and
second input strobe signals in the preamble time are
set a predetermined time before a first input data
5 item is received.

10 16. The electronic instrument as claimed
in claim 15, wherein transistors of a unit supplying
the input data to said memory device which
transistors drive the strobe signal lines are
controlled to be in a off state in a waiting time
15 period.

20 17. The electronic instrument as claimed
in claim 10, wherein each of cross points of the
first and second input strobe signals is set at an
edge trigger point of a corresponding one of input
data items.

25

30 18. The electronic instrument as claimed
in claim 10, wherein each of cross points of the
first and second input strobe signals is set at a
center point of a corresponding one of input data
items.

35

19. An electronic instrument comprising:
a memory device; and
strobe signal lines through which a first
output strobe signal and a second output strobe
5 signal are transmitted in synchronism with output
data from said memory device in a data output
operation and a first input strobe signal and a
second input strobe signal are transmitted in
synchronism with input data supplied to said memory
10 device in a data input operation, the first and
second output strobe signals being in complementary
relation to each other, the first and second input
strobe signals being in complementary relation to
each other.

15

20. The electronic instrument as claimed
in claim 19, said memory device comprises:
a strobe output buffer that generates the
first and second output strobe signals based on a
predetermined signal, the first and second output
strobe signals being supplied from said strobe
25 output buffer to said strobe signal lines when the
output data is output from said memory device; and
a strobe input buffer that receives the
first and second input strobe signals transmitted
through said strobe signal lines and generates,
30 based on the first and second input strobe signals,
a strobe clock signal used to settle input data
items supplied to said memory device.

35

21. The electronic instrument as claimed

in claim 19, wherein the first and second output
strobe signals have different levels in a first
preamble time which is a time period before a head
of a cross point train of the first and second
5 output strobe signals, the head of the cross point
corresponding to a start of a strobe period of the
first and second output strobe signals, and wherein
the first and second input strobe signals have
different levels in a second preamble time which is
10 a time period before a head of a cross point train
of the first and second input strobe signals, the
head of the cross point corresponding to a start of
a strobe period of the first and second input strobe
signals.

15

22. The electronic instrument as claimed
20 in claim 21, wherein the first and second output
strobe signals have different levels in a first
postamble time which is a time period after a cross
point of the first and second output strobe signals
which cross point corresponds to an end of a strobe
25 period of the first and second output strobe signals,
and wherein the first and second input strobe
signals have different levels in a second postamble
time which is a time period after a cross point of
the first and second input strobe signals which
30 cross point corresponds to an end of a strobe period
of the first and second input strobe signals.

35

23. The electronic instrument as claimed
in claim 22, wherein said strobe signal lines

includes output strobe signal lines through which
the first and second output strobe signals and input
strobe signal lines through which the first and
second input strobe signal lines, said output strobe
5 signal lines and said input strobe signal lines
being separated from each other, wherein when an
even number of consecutive output data items are
output, the levels of the first and second output
strobe signals are controlled in a waiting time
10 period to be maintained at the same levels as in the
first postamble time, and wherein when an even
number of consecutive input data items are supplied,
the levels of the first and second input strobe
signals are controlled in a waiting time period to
15 be maintained at the same levels as in the second
postamble time.

20

24. The electronic instrument as claimed
in claim 22, wherein said strobe signal lines
includes output strobe signal lines through which
the first and second output strobe signals and input
25 strobe signal lines through which the first and
second input strobe signal lines, said output strobe
signal lines and said input strobe signal lines
being separated from each other, wherein when an odd
number of consecutive data output items are output,
30 the levels of the first and second output strobe
signals are controlled in a waiting time period to
be maintained at the same levels as in the first
postamble time and then restored at the start of the
second preamble time in the next data read operation.

35

25. A semiconductor memory device provided in an electronic instrument having clock lines through which complementary clock signals are transmitted to be used for synchronization of a data
5 output operation for said semiconductor memory device, and strobe signal lines through which a first output strobe signal and a second output strobe signal are transmitted to be used to settle output data from said semiconductor memory device in
10 the data output operation, the first and second output strobe signals being in complementary relation to each other, said semiconductor memory device comprising:
15

a data output buffer that outputs the output data from a memory bank; and
a strobe output buffer that generates the first and second output strobe signals based on a predetermined signal, the first and second output strobe signals being supplied from said strobe
20 output buffer to said strobe signal lines when the output data is output from said data output buffer.

25

26. A semiconductor memory device provided in an electronic instrument having clock lines through which complementary clock signals are transmitted to be used for synchronization of a data
30 input operation for said semiconductor memory device, and strobe signal lines through which a first input strobe signal and a second input strobe signal are transmitted to be used to settle input data supplied to said semiconductor memory device in the data
35 input operation, the first and second input strobe signals being in complementary relation to each other, said semiconductor memory device comprising:

a strobe input buffer that receives the first and second input strobe signals transmitted through said strobe signal lines and generates a strobe clock signal based on the first and second
5 input strobe signals; and

a data input buffer that receives input data items supplied to said semiconductor memory device, the input data items being settled by using the clock strobe signal generated by said input
10 strobe buffer.

15 27. A semiconductor memory device provided in an electronic instrument having clock lines through which complementary clock signals are transmitted to be used for synchronization of a data output operation and a data input operation for said
20 semiconductor memory device, and strobe signal lines through which a first output strobe signal, a second output strobe signal, a first input strobe signal and a second input strobe signal are transmitted to be used to settle output data from said memory
25 device in the data output operation and to settle input data supplied to said semiconductor memory device, the first and second output strobe signals being in complementary relation to each other, the first and second input strobe signals being in
30 complementary relation to each other, said memory device comprising:

 a data output buffer that outputs the output data from a memory bank;

35 a strobe output buffer that generates the first and second output strobe signals based on a predetermined signal, the first and second output strobe signals being supplied from said strobe

output buffer to said strobe signal lines when the output data is output from said data output buffer;

5 a strobe input buffer that receives the first and second input strobe signals transmitted through said strobe signal lines and generates a strobe clock signal based on the first and second input strobe signals; and

10 a data input buffer that receives input data items supplied to said semiconductor memory device, the input data items being settled by using the clock strobe signal generated by said input strobe buffer.

ABSTRACT OF THE DISCLOSURES

An electronic instrument includes a memory device, clock lines through which complementary clock signals are transmitted to be used for synchronization of a data output operation and a data input operation for the memory device, and strobe signal lines through which a first output strobe signal, a second output strobe signal, a first input strobe signal and a second input strobe signal are transmitted to be used to settle output data from the memory device in the data output operation and to settle input data supplied to the memory device, the first and second output strobe signals being in complementary relation to each other, the first and second input strobe signals being in complementary relation to each other.

FIG.1

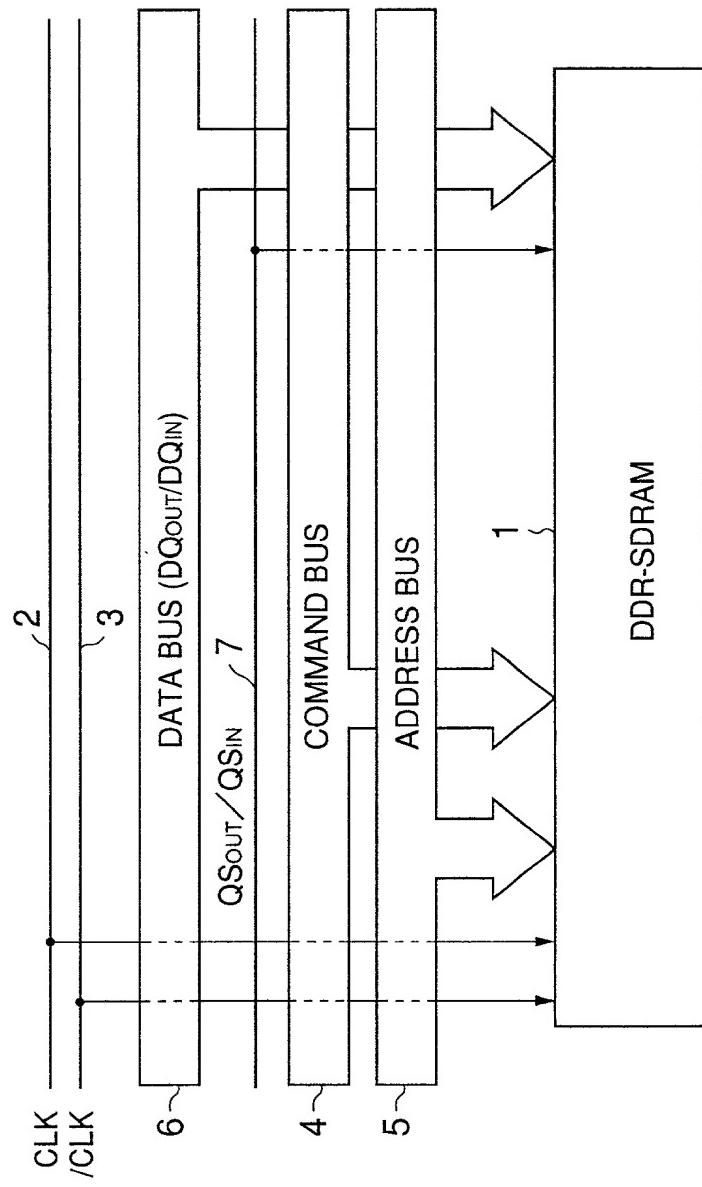


FIG.2

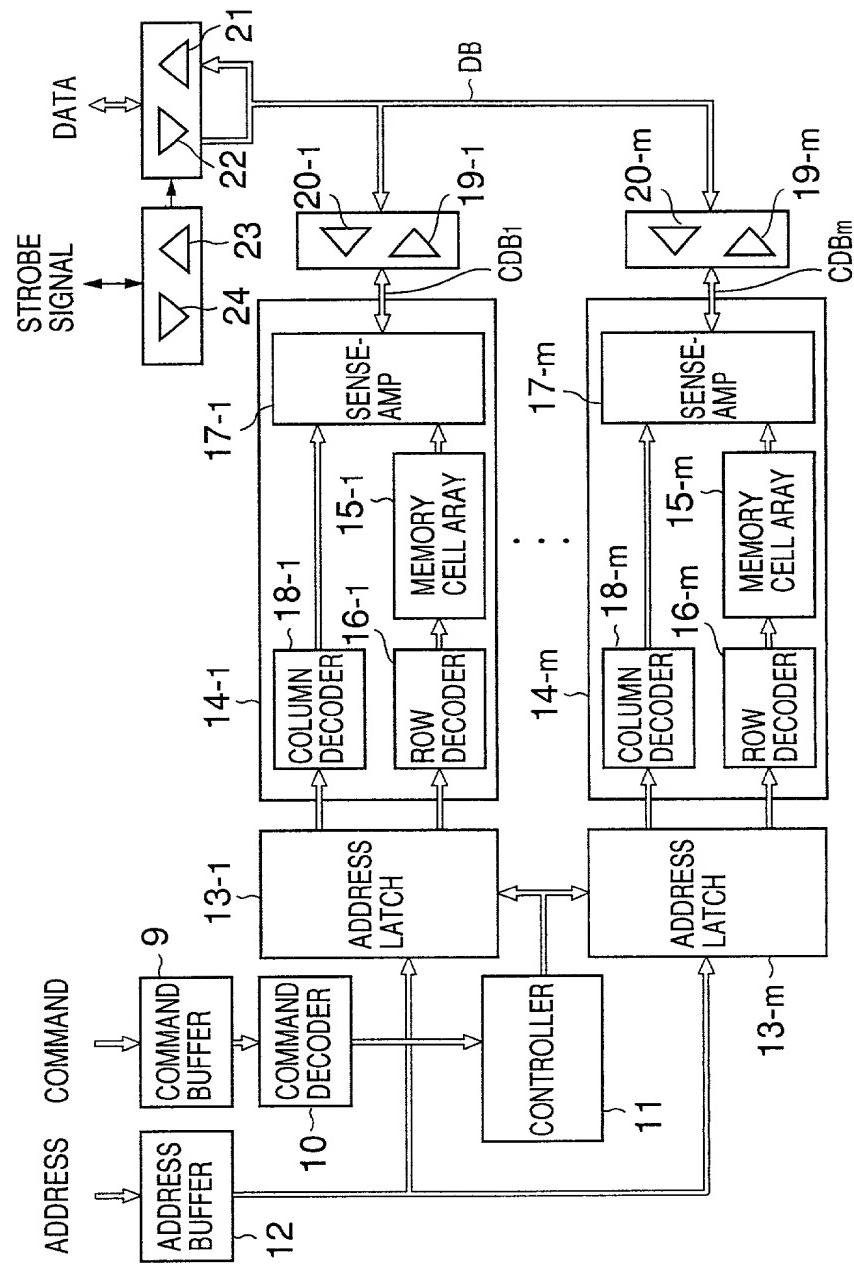
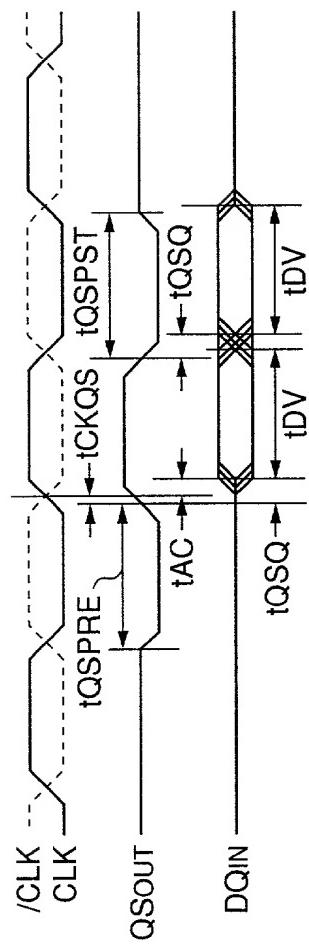
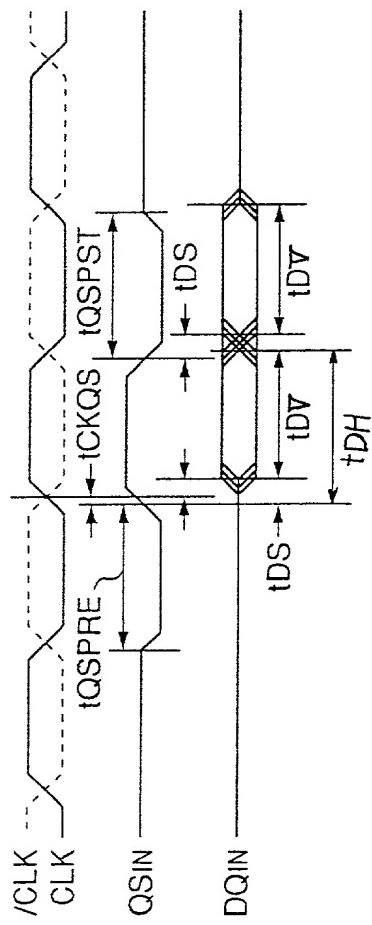


FIG.3



PARAMETERS	SYMBOL	PARAMETERS	SYMBOL
QS ACCESS TIME FROM CLK	tCKQS	DATA OUTPUT SKEW FROM QS	tQSQ
QS PREAMBLE TIME	tQSPRE	DATA ACCESS TIME FROM QS	tAC
QS POSTAMBLE TIME	tQSPST	DATA OUTPUT VALID TIME	tDV

FIG.4



PARAMETERS	SYMBOL	PARAMETERS	SYMBOL
QS ACCESS TIME FROM CLK	tCKQS	DATA INPUT SET UP TIME FROM QS	tD
QS PREAMBLE TIME	tQSPRE	DATA INPUT HOLD TIME FROM QS	tD
QS POSTAMBLE TIME	tQSPST	DATA VALID PERIOD	tDV

FIG.5

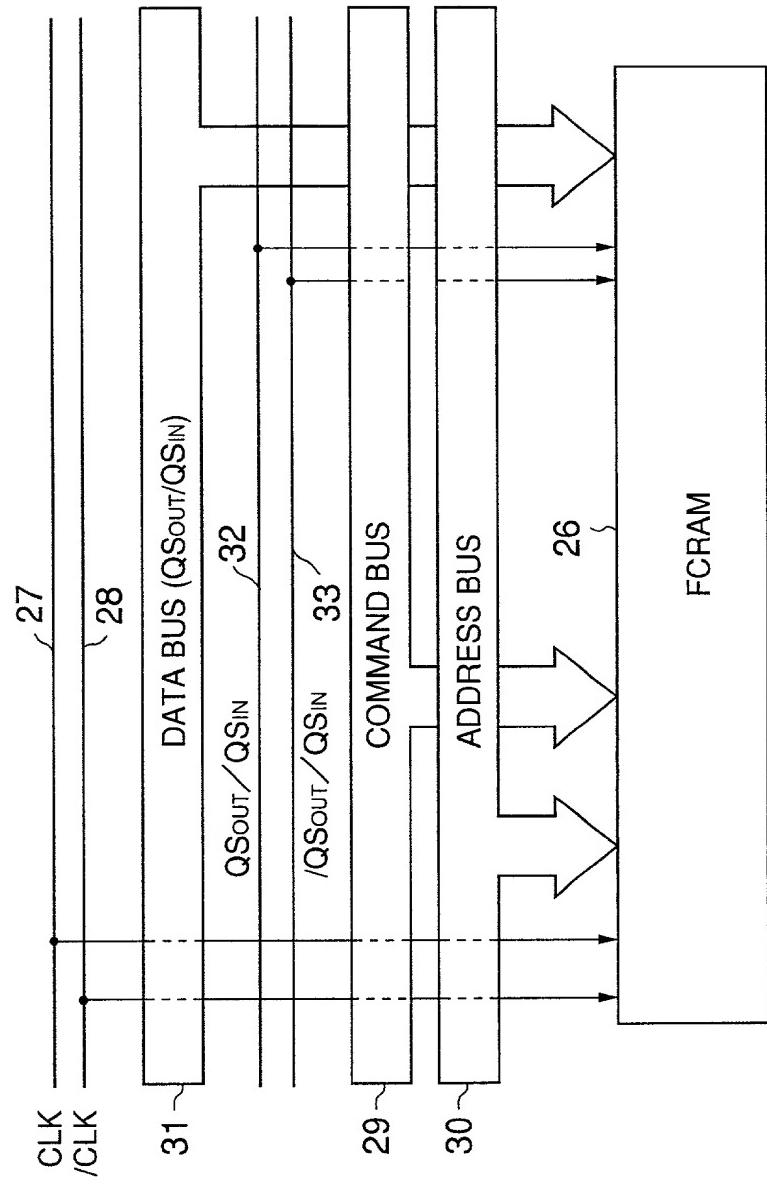


FIG.6

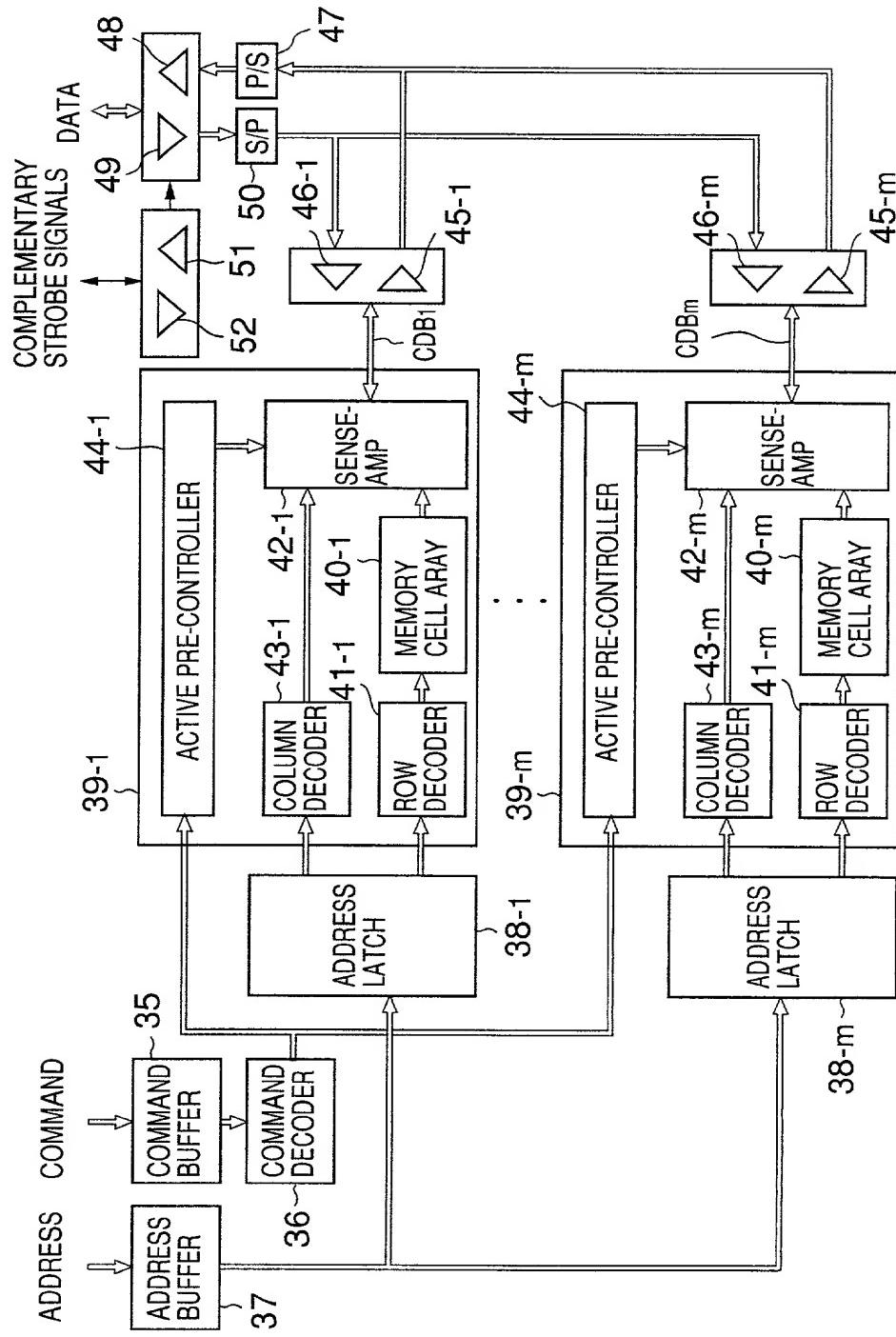


FIG.7

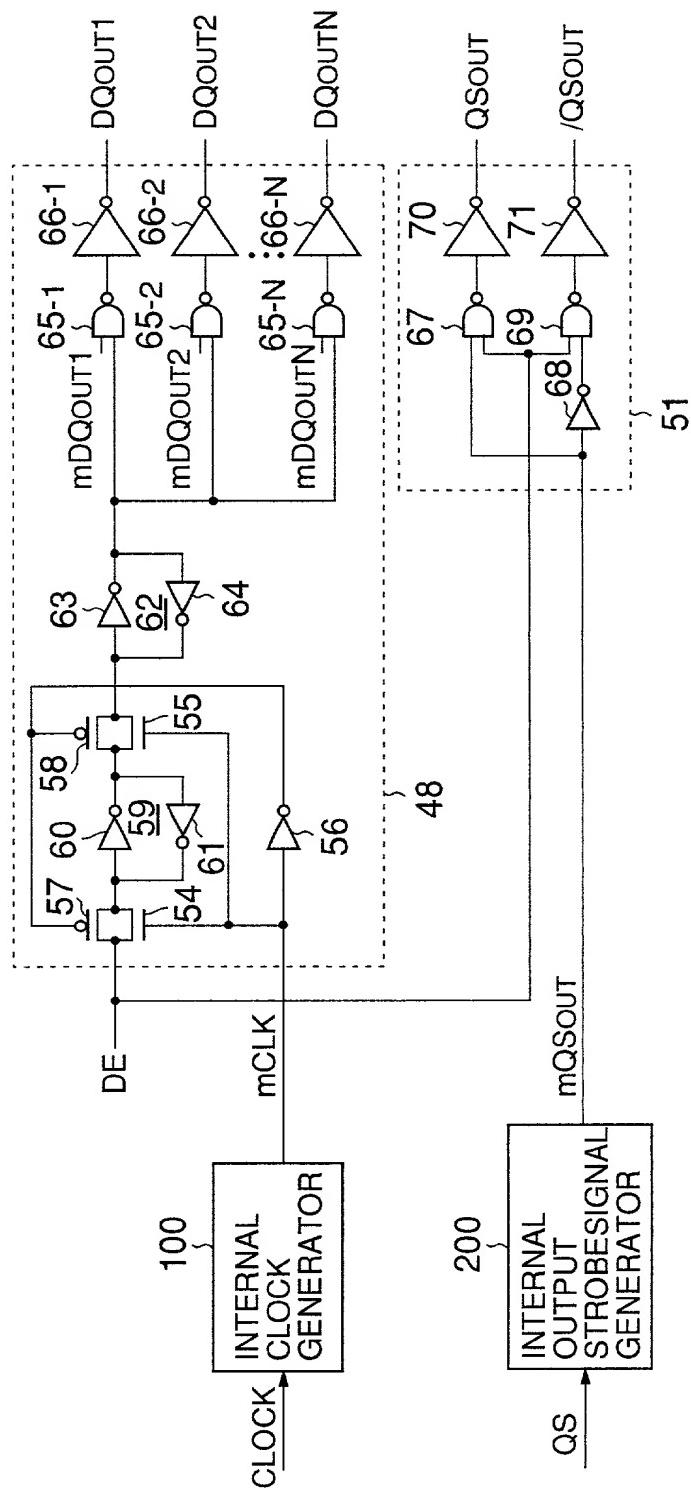


FIG.8

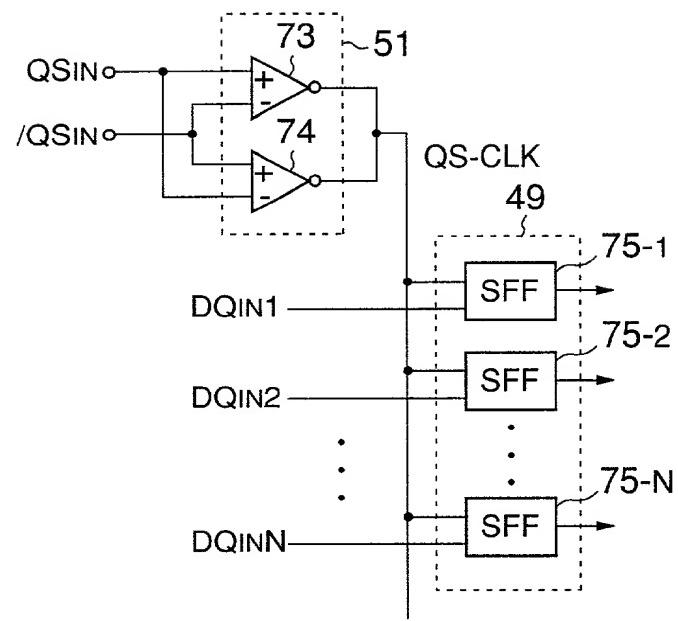
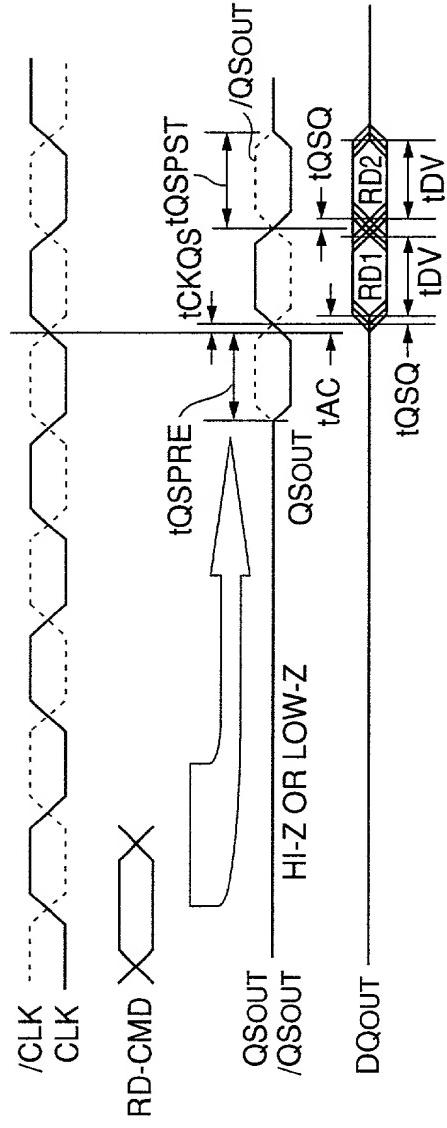


FIG.9



PARAMETERS	SYMBOL	PARAMETERS	SYMBOL
QS ACCESS TIME FROM CLK	tCKQS	DATA OUTPUT SKEW FROM QS	tQSQ
QS PREAMBLE TIME	tQSPRE	DATA ACCESS TIME FROM QS	tAC
QS POSTAMBLE TIME	tQSPST	DATA OUTPUT VALID TIME	tDV

FIG.10

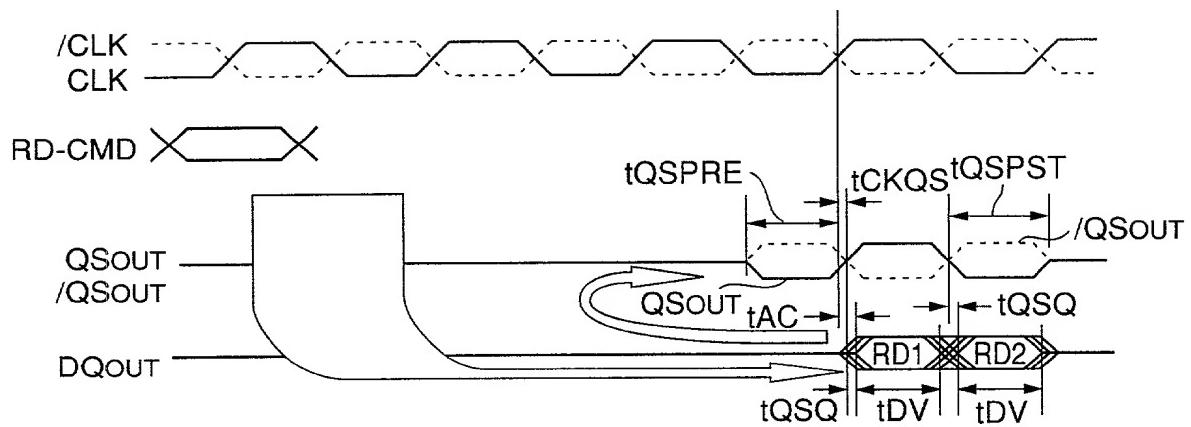


FIG.11

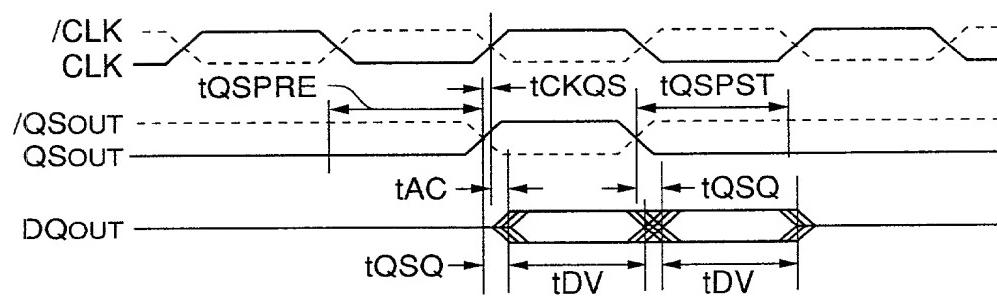


FIG.12

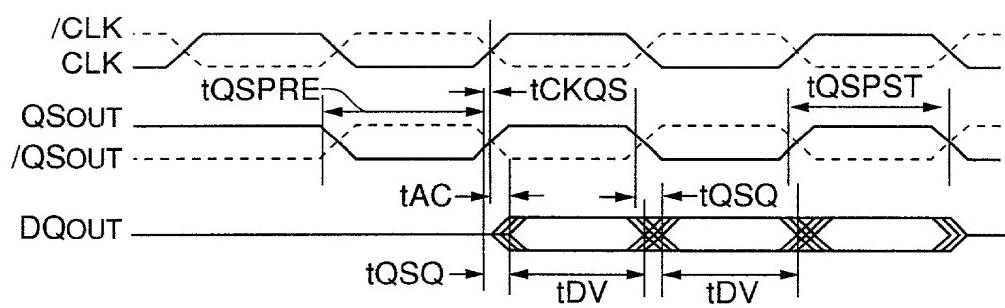


FIG.13

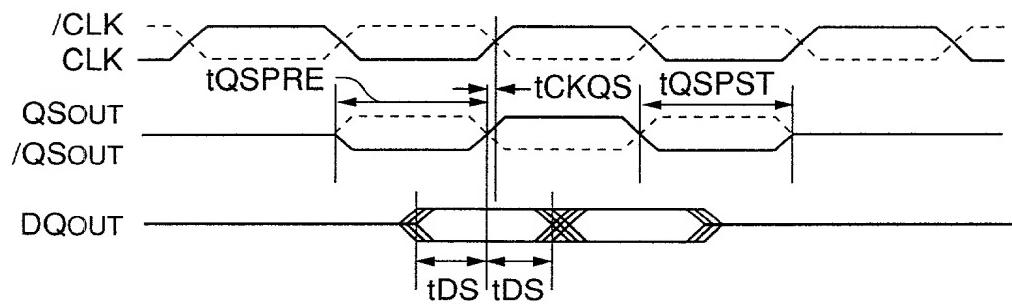
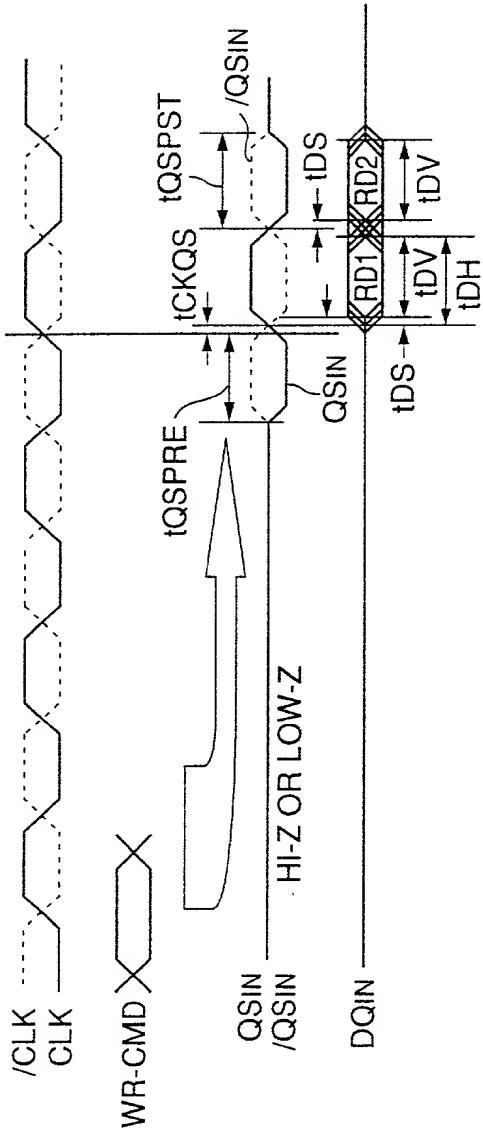


FIG. 14



PARAMETERS	SYMBOL	PARAMETERS	SYMBOL
QS ACCESS TIME FROM CLK	tCKQS	DATA INPUT SET UP FROM QS	tDS
QS PREAMBLE TIME	tQSPRE	DATA INPUT HOLD TIME FROM QS	tDH
QS POSTAMBLE TIME	tQSPST		

FIG.15

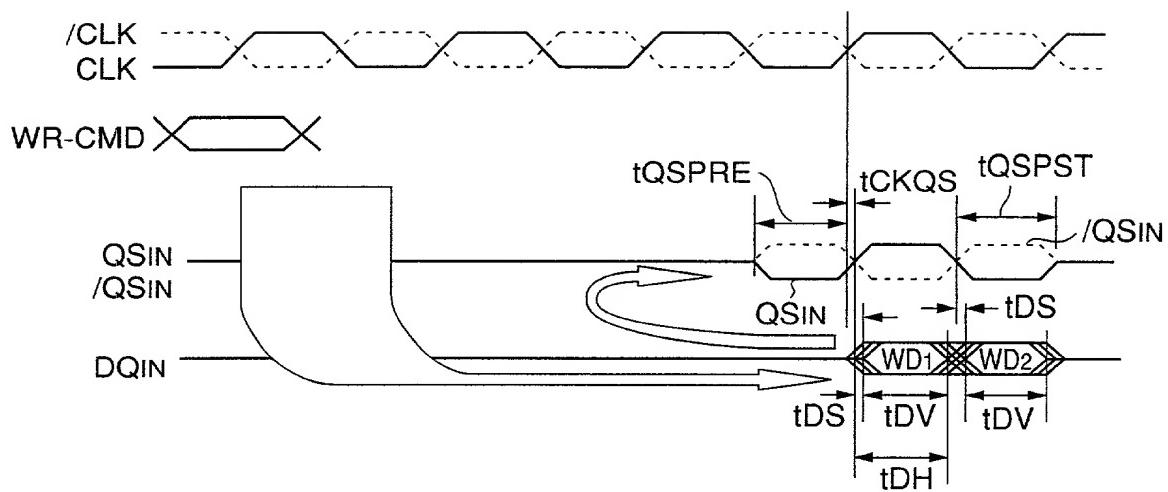


FIG.16

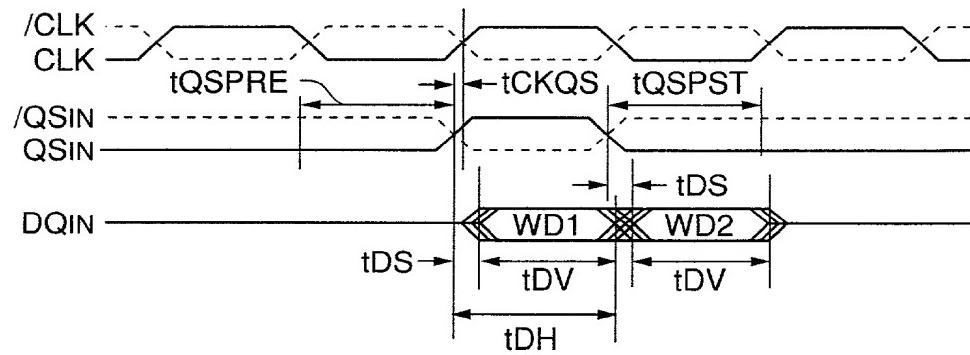


FIG.17

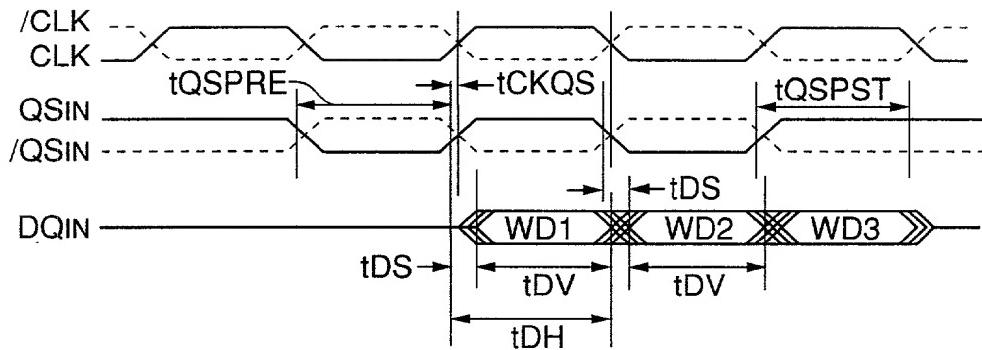
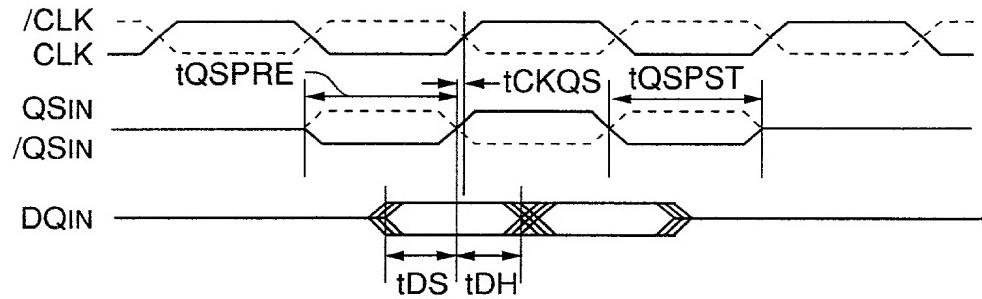


FIG.18



Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

ELECTRONIC INSTRUMENT AND SEMICONDUCTOR

MEMORY DEVICE

上記発明の明細書（下記の欄でX印がついていない場合は、本書に添付）は、

the specification of which is attached hereto unless the following box is checked:

- 一月一日に提出され、米国出願番号または特許協定条約国際出願番号を _____ とし、
(該当する場合) _____ に訂正されました。

was filed on _____
as United States Application Number or
PCT International Application Number
_____ and was amended on
_____ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第37編第1条56項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

Japanese Language Declaration

(日本語宣言書)

私は、米国法典第35編119条(a)-(d)項又は365条(b)項に基づき下記の、米国以外の国の少なくとも一ヵ国を指定している特許協力条約365(a)項に基づく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

Prior Foreign Application(s) (Patent Application)

外国での先行出願

No.10-178315

(Number)
(番号)

Japan

(Country)
(国名)(Number)
(番号)(Country)
(国名)

私は、第35編米国法典119条(e)項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

(Application No.)
(出願番号)(Filing Date)
(出願日)

私は、下記の米国法典第35編120条に基いて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約365条(c)に基づく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第35編112条第1項又は特許協力条約で規定された方で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国提出までの期間中に入手された、連邦規則法典第37編1条56項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

(Application No.)
(出願番号)(Filing Date)
(出願日)(Application No.)
(出願番号)(Filing Date)
(出願日)

私は、私自身の知識に基づいて本宣言書中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じるところに基づく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第18編第1001条に基づき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は既に許可された特許の有効性が失われるなどを認識し、よってここに上記のごとく宣誓を致します。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Priority Not Claimed

優先権主張なし

25/June/1998

(Day/Month/Year Filed)

(出願年月日)

(Day/Month/Year Filed)

(出願年月日)

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.)
(出願番号)(Filing Date)
(出願日)

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application.

(Status: Patented, Pending, Abandoned)
(現況: 特許許可済、係属中、放棄済)(Status: Patented, Pending, Abandoned)
(現況: 特許許可済、係属中、放棄済)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration

(日本語宣言書)

委任状： 私は下記の発明者として、本出願に関する一切の手続を米特許商標局に対して遂行する弁護士または代理人として、下記の者を指名いたします。（弁護士、または代理人の氏名及び登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (list name and registration number)

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